DSP Performance Comparison - TI 6414 versus TI 6203

using the RodDemo

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Direct comparison between the two DSPs using the existing hardware:

- The 6203-based PU board (available since July 2001) using a 300 MHz 6203 CPU;
- The 6414-based PU board (available since February 2002) using a 600 MHz 6414 CPU.

For this test, the two boards are providing the same functionality:

- Input event buffering: 64 events
- Output event buffering: 4 events
- Optimal filtering: calculate E, t, chi2 for all channels, with same precision (see later)
  Code is either loop26 (for 6203 and 6414) or loop16 (optimized for the 6414)
- Histogramming: fill log(E) and t histograms independently for each channel and for each gain. All histograms have 128 bins. Bins for high gain are 32-bit numbers, while bins for medium and low gain are packed together to form a 32-bit word: N-bit numbers for medium gain, (32-N)-bit numbers for low gain.
  The bin definition (granularity) can be configured so that any 7 bits of log(E) and t are mapped to the histogram. The finest granularity of t is 4 ps.
  log(E) is understood as composed of all (4) bits of the E exponent (in its floating-point representation) followed by the most significant (3) bits of the E fraction: $E = 2^m \times 1.f$
Optimal filtering implementation

- Using 16-bit signed weights and 32-bit baseline subtraction for E and E*t calculation.
- Energy result absolute scale is precise to $\delta E = 2^{-15}$ ADC counts (baseline quantization error)
- Relative precision $\delta E/E = 2^{-16}$ (weights quantization error)
- Weights are set to give E in ADC counts (for loop26) or $2^{15} \times$ ADC counts (loop16)
- Time lsb = 4 ps with dynamic range of 14 bits (loop26) or 16 bits (loop16).
- $\chi^2$ is in ADC$^2$ stored in 16 bits.
DSP time resolution

32-bit time (intermediate result)

E (adc)

t (ns)

16-bit time (final result, truncated from 32-bit)
For the 6203 and the 6414:

- **loop26** computes and stores the energy in floating-point format; \( t, c^2 \) and the gain bits packed together in a 32-bit word. Needs 13 6203 cycles per channel;
- intermediate step to **flag channels** above a given threshold and fill a channel mask (four 32-bit words). Needs 0.5 6203 cycles per channel;
- **histogramming** of \( \log(E) \) and \( t \), and **suppression** of \( t, c^2 \) for channels below threshold. Needs 6 (6203) cycles per channel above threshold, plus a small overhead. The 6203 code has been slightly modified to remove a cross-path stall which would occur on the 6414.

For the 6414:

- **loop16** computes and stores the energy in fixed-point format; \( t \) and \( c^2 \) are packed in a 32-bit word; the gains are stored separately.

The **loop16** code was developed in August 2001. It is designed to perform exactly the same computation as **loop26** (except conversion of \( E \) to floating-point) and is **optimized for best performance on the 6414** (memory accesses, L1D miss pipelining). This code has been recently tested on the existing hardware.

- **histogramming** of \( \log(E) \) and \( t \), and **suppression** of \( t, c^2 \) for channels below threshold. There is no intermediate step (mask filling) between **loop16** and histogramming. This code needs 6 cycles for each of the 128 channels, plus any additional stall cycles due to the 6414 cache. There are no cross-path stalls or bank conflicts.
Other details

- Histogramming of $\log(E)$ and $t$ is done only for channels above user-specified thresholds (one for $\log(E)$ and one for $t$). For the comparison, both thresholds (as well as the threshold for storing $t$, $\chi^2$) have been set to 1.9 ADC counts.

  This way, the number of channels histogrammed fluctuates event by event.

- The data are downloaded to the DSP via the host-port interface, 64 events at a time (the size of the DSP input buffer) after which a command is sent to the DSP to process all 64 events. The DSP only performs the computation and the output DMA to write the data to the FIFO.

- The **processing time** is **measured event by event** by using the DSP counter. On the 6203, the counter increments at 1/4 of the CPU clock rate (75 MHz). On the 6414, it increments at 1/8 of the CPU clock rate (also 75 MHz).

  The counter values are stored in the output data header, and read out via VME along with the results of the computation.

- The **FEB data set** used is taken from a combination of free-gain testbeam runs (300 GeV position scan).

  The “optimal filtering” weights use dummy (analytical) pulse shapes, typical for middle-sampling cells. However the true noise autocorrelation and pedestals are taken into account.

  The results of the DSP calculation are compared, event by event, to full-precision (double precision) calculation done offline, using the same weights.
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Conclusion

- On the 6414, loop16 alone is (as expected from simulation) twice faster than loop26.
- On the 600 MHz 6414, loop16 (alone) is twice faster than loop26 on the 300 MHz 6203.
- However, on the 6414, histogramming (and therefore overall) performance degrades as the number of channels for which histograms are filled, increases.
  
  This degradation is faster than predicted by the simulation.
  When log(E) and t histograms are filled for all channels, the two DSPs show similar performance.

- Nevertheless, if histograms are filled for only a (small) fraction of the events, or for just the channels above some E threshold, then the 6414 will be faster than the 6203.