PU Operation in Staging Mode

In December 2001 we proposed to allow a DSP to handle data from 2 FEBs, with no I/O bandwidth limitation. The L1A trigger rate will be limited solely by the DSP computing power (staging mode).

This can be achieved with a different connector arrangement, and by utilizing a larger device (1k100 instead of 1k50) for the PU Input FPGA.

In order to fully test this scenario, the 6414 Demo board is already equipped with the larger device.

In particular, for the Front-End Crate test, the readout will be in “staged mode” using the 6414 Demo boards provided by LAPP.

The 1k100 Input FPGA code needed to handle two FEBs has been developed and tested at Nevis.
During normal data taking, to achieve best possible CPU performance of the DSP, it is necessary to rearrange the FEB data according to the DSP algorithm requirements.

For this, 4 complete FEB events must fit within the Input FPGA memory (staged mode).

In the Input FPGA, the data streams for each FEB are kept totally independent.

The 1k100 internal memory allows to satisfy the above requirements provided that no more than 7 ADC samples are read out.

The code developed at Nevis performs complete error checking, and data rearrangement as needed by the loop16 optimal filtering code. The rearranged data are presented to the DSP at full bandwidth of the 64-bit memory bus @ 100 MHz.

Only 60% of the logic resources of the 1k100 are used.

Fastest EMIF clock is 117.6 MHz for 1k100-2 (the target is 100 MHz).
5 events with 5 samples, auto gain (loop16 rearrangement)

FEB1 events to DSP (EMIFA CE2)

FEB2 events to DSP (EMIFA CE3)
For debugging, it will be required to read out events with any number of samples and/or gains. Large events cannot fit entirely in the FPGA memory (even for a 20k device) and therefore a different approach (different FPGA code) must be used.

In this mode, ADC data are transferred to the DSP as soon as received from the FEB, sample-by-sample. The FPGA simply behaves as two parallel FIFOs, one FIFO for each FEB.

However, to continue to perform error detection on the incoming data (parity checking etc.) the FPGA must be provided with the number of samples and the number of gains read out. This is done by writing a register inside the Input FPGA.

For running in this mode, the Input FPGA code is even simpler than for data rearrangement. Only 66% of the memory (8 out of 12 EABs) and only 55% of the logic cells are used, for a 1k100 device.
One event with 9 samples, 1 gain, no data rearrangement

Stefan Simion for Nevis Labs, Columbia University and the U.S. ROD group.
One event with 9 samples, 2 gains, no data rearrangement.
One event with 9 samples, 3 gains, no data rearrangement.
Conclusion

Two-FEB read-out is operational and will be used in the system crate test.

The 1k100 device is adequate for staging-mode data taking:

- All known functional requirements are satisfied.
- Reasonable room left for unforeseen additions.

Summary of 1k100 resources used:

- all 12 EABs, 60% of logic cells for fully-flexible data rearrangement (up to 7 samples).
- 8 EABs, 55% of logic cells for debugging mode (any number of samples/gains).